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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,252	03/24/2004	Masanori Takeuchi	122.1588	4082
21171 STAAS & UA1	7590 07/31/2007	EXAMINER		
STAAS & HALSEY LLP SUITE 700			DHARIA, PRABODH M	
1201 NEW YC WASHINGTO	ORK AVENUE, N.W. N, DC 20005		ART UNIT	PAPER NUMBER
,			2629	
			MAIL DATE DELIVERY MODE	
			MAIL DATE 07/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		Application No.	Applicant(s)			
Office Action Summary		10/807,252	TAKEUCHI ET AL.			
		Examiner	Art Unit			
		Prabodh M. Dharia	2629			
Period fo	The MAILING DATE of this communication ap	ppears on the cover sheet w	ith the correspondence address			
A SHOWHIC - Exter after - If NO - Failu Any r earne	ORTENED STATUTORY PERIOD FOR REPLICHEVER IS LONGER, FROM THE MAILING Designs of time may be available under the provisions of 37 CFR 1. SIX (6) MONTHS from the mailing date of this communication. Operiod for reply is specified above, the maximum statutory period re to reply within the set or extended period for reply will, by statuted the reply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNION (136(a). In no event, however, may a red will apply and will expire SIX (6) MON te, cause the application to become AE	CATION. reply be timely filed WTHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).			
Status						
1)⊠	Responsive to communication(s) filed on <u>24 March 2004</u> .					
2a) <u></u> □	a) This action is FINAL . 2b) This action is non-final.					
3)	,—					
	closed in accordance with the practice under	Ex parte Quayle, 1935 C.D.). 11, 453 O.G. 213.			
Dispositi	on of Claims					
5) 6) 7)	Claim(s) 1-56 is/are pending in the application 4a) Of the above claim(s) is/are withdra Claim(s) is/are allowed. Claim(s) is/are rejected. Claim(s) is/are objected to. Claim(s) 1-56 are subject to restriction and/or	awn from consideration.				
Applicati	on Papers					
9)	The specification is objected to by the Examin	er.				
10)⊠	The drawing(s) filed on 24 March 2004 is/are:	a)⊠ accepted or b)⊡ obj	jected to by the Examiner.			
	Applicant may not request that any objection to the					
11)	Replacement drawing sheet(s) including the correct The oath or declaration is objected to by the E	· · · · · · · · · · · · · · · · · · ·	-			
Priority u	ınder 35 U.S.C. § 119					
a)[Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority document application from the International Burea See the attached detailed Office action for a list	nts have been received. nts have been received in A ority documents have been au (PCT Rule 17.2(a)).	Application No received in this National Stage			
Attachmen						
2) Notice	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO/SB/08) er No(s)/Mail Date 03-24-2004.	Paper No(Summary (PTO-413) s)/Mail Date informal Patent Application			

DETAILED ACTION

Election/Restrictions

1. Restriction is required under 35 U.S.C. 121 and 372.

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

In accordance with 37 CFR 1.499, applicant is required, in reply to this action, to elect a single invention to which the claims must be restricted.

2. Status: Receipt is acknowledged of papers submitted on 03-24-2004 under new application, which have been placed of record in the file. Claims 1-56 are pending in this action.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 03-24-2004 is in compliance 3. with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner. PTO 1449 initialed and signed by examiner are attached.

Election/Restrictions

- Restriction to one of the following inventions is required under 35 U.S.C. 121: 4.
 - Claims 1-14 are drawn to a display apparatus which expresses luminance by I. varying light emission time length and displays gray scale by using a subfield method with a gain control circuit compressing the number of gray scale levels of

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an input signal and an error diffusion circuit receiving intermediate image signal and increasing the number of gray scale levels by simulating additional gray scale levels through error diffusion, classified in class 345, subclass 694 and 313 subclass 503 and 235, subclass 462.42.

- II. Claims 15-28 are drawn to a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method has multiple path to generate multiple image signal of a image in motion using switching control from an input image signal and with a gain control circuit compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving an output image signal from sub gain control circuit and outputting first image signal through error diffusion process, classified in class 345, subclass 204, 600, subclass 173, 701, subclass 211.
- Claims 29-42 are drawn to a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method by compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving intermediate image signal and generating output image signal through error diffusion process, classified in class 382, subclass 264, and 345, subclass 76.

Claims 43-56 are drawn to a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method has multiple path to generate multiple image signal of a image in motion using switching control from an input image signal and with a computational process compressing the number of gray scale levels of an input signal and an error diffusion applied to sub gain control circuit and generating first image signal through error diffusion process, classified in class 345, subclass 596, 345, subclass 600, and 345, subclass 163.

5. The inventions are distinct, each from other because:

Invention I relates to a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method with a gain control circuit compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving intermediate image signal and increasing the number of gray scale levels by simulating additional gray scale levels through error diffusion; however, it does not relate to a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method has multiple path to generate multiple image signal of a image in motion using switching control from an input image signal and with a gain control circuit or computational process compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving an output image signal from sub gain control circuit and outputting first image signal through error diffusion process; a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield

method by compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving intermediate image signal and generating output image signal through error diffusion process; and a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method has multiple path to generate multiple image signal of a image in motion using switching control from an input image signal and with a computational process compressing the number of gray scale levels of an input signal and an error diffusion applied to sub gain control circuit and generating first image signal through error diffusion process.

Invention II relates relate to a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method has multiple path to generate multiple image signal of a image in motion using switching control from an input image signal and with a gain control circuit compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving an output image signal from sub gain control circuit and outputting first image signal through error diffusion process; however, it does not relate to a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method by compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving intermediate image signal and generating output image signal through error diffusion process; a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method has multiple path to generate multiple image signal of a image in motion using switching control from an input image signal and with a computational process compressing the

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number of gray scale levels of an input signal and an error diffusion applied to sub gain control circuit and generating first image signal through error diffusion process; and a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method with a gain control circuit compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving intermediate image signal and increasing the number of gray scale levels by simulating additional gray scale levels through error diffusion.

Invention III relates to a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method by compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving intermediate image signal and generating output image signal through error diffusion process; however, it does not relate to a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method has multiple path to generate multiple image signal of a image in motion using switching control from an input image signal and with a computational process compressing the number of gray scale levels of an input signal and an error diffusion applied to sub gain control circuit and generating first image signal through error diffusion process; a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method with a gain control circuit compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving intermediate image signal and increasing the number of gray scale levels by simulating additional gray scale levels through error diffusion; and a display apparatus which

expresses luminance by varying light emission time length and displays gray scale by using a subfield method has multiple path to generate multiple image signal of a image in motion using switching control from an input image signal and with a gain control circuit compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving an output image signal from sub gain control circuit and outputting first image signal through error diffusion process.

Invention IV relates to a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method has multiple path to generate multiple image signal of a image in motion using switching control from an input image signal and with a computational process compressing the number of gray scale levels of an input signal and an error diffusion applied to sub gain control circuit and generating first image signal through error diffusion process however, it does not relate to a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method with a gain control circuit compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving intermediate image signal and increasing the number of gray scale levels by simulating additional gray scale levels through error diffusion; a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method has multiple path to generate multiple image signal of a image in motion using switching control from an input image signal and with a gain control circuit compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving an output image signal from sub gain control circuit and outputting first image signal

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through error diffusion process; and a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method by compressing the number of gray scale levels of an input signal and an error diffusion circuit receiving intermediate image signal and generating output image signal through error diffusion process.

- 6. These above, mentioned reasons the inventions described and categorized by class /subclass above are distinct. Search required for each class and subclass is independent.
- 7. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.
- 8. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement is traversed (37 CFR 1.143).

Conclusion

- 9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.
- 10. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Prabodh Dharia

Full Signatory Authority Program

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July 21, 2007